

What is claimed:

1 1. A method for manufacturing a semiconductor device, the method comprising:
2 (a) forming a gate dielectric layer over a semiconductor substrate;
3 (b) forming a gate electrode over the gate dielectric layer;
4 (c) forming an extension control layer over the semiconductor substrate on sides of
5 the gate dielectric layer; and
6 (d) forming a first impurity layer and a second impurity layer by ion-implanting an
7 impurity in the semiconductor substrate,
8 wherein an extension region is formed in the semiconductor substrate below the
9 extension control layer during the ion-implanting used to form the first impurity layer and
10 the second impurity layer.

1 2. A method for manufacturing a semiconductor device according to claim 1,
2 wherein the step (c) further includes the step of forming a sidewall protection film on
3 sidewalls of the gate electrode with the extension control layers.

1 3. A method for manufacturing a semiconductor device according to claim 2,
2 wherein the step (c) further includes the steps of:
3 (c - 1) forming a dielectric layer over the semiconductor substrate; *1/2 1st paragr. ph*
4 (c - 2) forming a sidewall mask layer on sides of the gate electrode over the
5 dielectric layer;
6 (c - 3) removing the dielectric layer using the sidewall mask layer as a mask to form
7 the extension control layer and the sidewall protection layer; and
8 (c - 4) removing the sidewall mask layer after the step (c - 3).

1 4. A method for manufacturing a semiconductor device according to claim 3,
2 wherein the extension control layer is formed from a material comprising silicon nitride.

1 5. A method for manufacturing a semiconductor device according to claim 4,
2 wherein the sidewall mask layer is formed from a material comprising silicon oxide.

1 6. A method for manufacturing a semiconductor device according to claim 3,
2 wherein the extension control layer is formed from a material comprising silicon oxide.

1 7. A method for manufacturing a semiconductor device according to claim 6,
2 wherein the sidewall mask layer is formed from a material comprising silicon nitride.

1 8. A method for manufacturing a semiconductor device according to claim 1,
2 wherein the extension control layer has a thickness of 5 – 50 nm.

1 9. A method for manufacturing a semiconductor device according to claim 3,
2 wherein the sidewall mask layer is formed to a thickness of 30 – 200 nm.

1 10. A semiconductor device comprising:
2 a gate dielectric layer provided over a semiconductor substrate;
3 a gate electrode provided over the gate dielectric layer;
4 a first impurity layer and a second impurity layer provided in the semiconductor
5 substrate and spaced away from sides of the gate dielectric layer;
6 an extension region provided in the semiconductor substrate between the gate
7 dielectric layer and at least one of the first impurity layer and the second impurity layer; and
8 an extension control layer provided over the extension region.

1 11. A semiconductor device according to claim 10, further comprising a sidewall
2 protection film formed on sidewalls of the gate electrode.

1 12. A semiconductor device according to claim 11, wherein the sidewall
2 protection film comprises silicon oxide and the extension control layer comprises silicon
3 nitride.

1 13. A semiconductor device according to claim 11, wherein the sidewall
2 protection film comprises silicon nitride and the extension control layer comprises silicon
3 oxide.

1 14. A semiconductor device according to claim 11, wherein the sidewall
2 protection film is integral with the extension control layer.

1 15. A semiconductor device according to claim 11, wherein the extension
2 control layer and the sidewall protection film define a substantially L-shaped cross-sectional
3 configuration.

1 16. A semiconductor device according to claim 10, wherein the extension control
2 layer comprises silicon nitride.

1 17. A semiconductor device according to claim 10, wherein the extension control
2 layer comprises silicon oxide.

1 18. A semiconductor device according to claim 10, wherein the extension control
2 layer has a thickness of 5 – 50 nm.

1 19. A semiconductor device according to claim 10, wherein the extension region
2 includes portions provided in the semiconductor substrate between the gate dielectric layer
3 and both the first impurity layer and the second impurity layer.

1 20. A semiconductor device according to claim 19, further comprising a sidewall
2 protection film on sidewalls of the gate electrode, wherein the extension control layer and
3 sidewall protection film form a substantially L-shaped structure in cross section on at least
4 one side of the gate dielectric layer.

1 21. A method for manufacturing a semiconductor device including extension
2 regions and source/drain regions formed using a single ion-implantation step, the method
3 comprising:
4 forming a gate dielectric layer over a semiconductor substrate;
5 forming a gate electrode over the gate dielectric layer;
6 forming extension control structures over a portion of the semiconductor substrate
7 next to the gate dielectric layer; and
8 a single ion-implanting step that forms extension regions in the semiconductor
9 substrate under the extension control structures and source/drain regions in the
10 semiconductor substrate adjacent to the extension layer, wherein the extension regions have
11 a depth that is less than that of the source/drain regions.

1 22. A method according to claim 21, further comprising forming sidewall
2 protection structures on sidewalls of the gate electrode, wherein the sidewall protection
3 structures are formed from the same material as the extension control structures.

1 23. A method according to claim 22, wherein the extension control structures and
2 sidewall protection structures are formed using a method comprising:
3 depositing a dielectric layer over the surface of the semiconductor substrate and the
4 gate electrode;
5 forming a mask layer on the dielectric layer;
6 anisotropically etching the mask layer to form a sidewall mask layer;
7 etching the dielectric layer using the sidewall mask layer as a mask so that the
8 dielectric layer remains at sidewalls of the gate electrode and extends a distance outward
9 from the gate dielectric layer along the surface of the dielectric layer; and
10 removing the sidewall mask layer;
11 wherein the dielectric layer remaining at sidewalls of the gate electrode defines the
12 sidewall protection structures and the dielectric layer extending a distance outward from the

13 gate dielectric layer along the surface of the dielectric layer defines the extension control
14 structures.

24. A method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from a dielectric material.

add 3
at 3